EE3043 Computer Architecture

Semester 241

Design of a Single Cycle RISC-V Processor

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# Introduction

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# Design Strategy

## Overview

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## ALU

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### Specification

| **Signal** | **Width** | **Direction** | **Description** |
| --- | --- | --- | --- |
|  |  |  |  |

## BRU

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### Specification

| **Signal** | **Width** | **Direction** | **Description** |
| --- | --- | --- | --- |
|  |  |  |  |

# Verification Strategy

## ALU

# Alternative Design

# Evaluation

# Result

## Quartus

| Logic Utilization/Total logic elements | xxx | xxx% |
| --- | --- | --- |

# 

# References

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